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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,437	07/26/2001	Sang Hoo Dhong	AUS9-2001-0301US1	7370

35236 7590 06/30/2006

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,437	DHONG ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the response filed on 04/12/06. The applicant argument regarding Yee et al are not persuasive; therefore, all the rejections based on Yee et al are retained and repeated for the following reasons.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yee et al., "Dynamic Logic Synthesis," IEEE, 1997, pp 345-348.

3. As to claims 1, 8, 13, and 14 Yee et al. teach a method of designing a logic circuit to provide a predetermined logical operation, the method including the steps of: (a) defining a logic synthesis block comprising a dynamic logic circuit (see fig 7 pp 345); (b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit (see fig 3-5), the logic synthesis being performed utilizing a synthesis library constrained to the logic synthesis block (see fig 1-8 pp 345-347 fig 4-5 dynamic gate); (c) eliminating unused devices in the intermediate circuit to produce a final circuit (see fig 1 fig 7 fig 8 pp 347, paragraph V. (MCNC combination benchmark Circuit), 1st paragraph); and (d) sizing the devices in the final circuit (see fig 1 fig 7 fig 8 pp 347 paragraph IV. (Synthesis of CD Domino Circuits), second paragraph).

4. As to claim 2, 9, and 15 Yee et al. teach wherein the step of defining the logic synthesis block includes selecting the largest practical dynamic AND/OR circuit for the integrated circuit fabrication technology in which the circuit is to be implemented (see fig 8 pp 347).

5. As to claim 3, 10, and 16 Yee et al. teach wherein the logic synthesis block comprises a four high and four wide dynamic AND/OR circuit (see fig 8 pp 347).

6. As to claim 4, 11, and 17 Yee et al. teach wherein the step of performing logic synthesis includes leaving the size of the devices in the logic synthesis block substantially unconstrained (see fig 1 fig 7 fig 8 pp 347).

7. As to claim 5, Yee et al. teach wherein the step of eliminating unused devices from the intermediate circuit includes detecting devices having a state that remains constant as the intermediate circuit operates to provide the predetermined logical operation (see fig 2-6 and fig 8 pp 346-347).

8. As to claim 6, Yee et al. teach wherein the step of sizing the devices in the final circuit includes analyzing the final circuit to determine the characteristics of each device in the final circuit necessary in order to consistently provide the predetermined logical operation and meet drive requirements (see fig 1-8 pp 345-347).

As to claim 7, 12, and 18 Yee et al. teach wherein the logic synthesis block uses a single activation/reset clock signal (see fig 2-6 and fig 8 pp 345-347).

Response to Amendment and Arguments

Applicant's arguments filed December 17th, 2004 have been fully considered but they are not persuasive.

Applicant contends that Yee et al do not describe "a method of designing a logic circuit to provide a predetermined logical operation, the method including the steps of: (a) defining a logic synthesis block comprising a dynamic logic circuit (see fig 7 pp 345); (b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis being performed utilizing a synthesis library constrained to the logic synthesis block; (c) eliminating unused devices in the intermediate circuit to produce a final circuit; and (d) sizing the devices in the final circuit" probes as claimed. In response to Applicant's argument that Yee et al do not describe "a method of designing a logic circuit to provide a predetermined logical operation, the method including the steps of: (a) defining a logic synthesis block comprising a dynamic logic circuit (see fig 7 pp 345); (b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit (see fig 3-5), the logic synthesis being performed utilizing a synthesis library constrained to the logic synthesis block (see fig 1-8 pp 345-347 fig 4-5 dynamic gate); (c) eliminating unused devices in the intermediate circuit to produce a final circuit (see fig 1 fig 7 fig 8 pp 347, paragraph V. (MCNC combination benchmark Circuit), 1st paragraph); and (d) sizing the devices in the final circuit (see fig 1 fig 7 fig 8 pp 347 paragraph IV. (Synthesis of CD Domino Circuits), second paragraph)". For this reason, examiner holds the rejection proper.

Applicant contends that Yee et al do not describe "A method of synthesizing a logic circuit to provide a predetermined logic operation, the method including the step of : defining a logic synthesis block comprising a single dynamic logic circuit" probes as claimed. In response to Applicant's argument that Yee et al do not describe "A method of synthesizing a logic circuit to provide a predetermined logic operation, the method including the step of : defining a logic

synthesis block comprising a single dynamic logic circuit" (see fig 4 fig 5 page 346 paragraph second to page 347 paragraph fourth). For this reason, examiner holds the rejection proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BINH TAT
Art Unit 2825
June 22, 2006

THUAN DO
Primary examiner-
06/26/06